RC5055

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors, Vtt and Clock Linear Regulator

Features

- Current Sensing is achieved using MOSFET $R_{DS(ON)}$
- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical at full load
- Adjustable operation from 50KHz to 1MHz
- Integrated Power Good and Enable/Soft Start functions
- Overvoltage protection pin controls external SCR
- Short circuit protection with current limiting
- Drives N-channel MOSFETs
- 24 pin SSOP package
- Meets Intel Pentium II specifications using minimum number of external components
- On board LDO for GTL termination
- On board LDO for Clock power supply
- TTL Compatible inputs

Applications

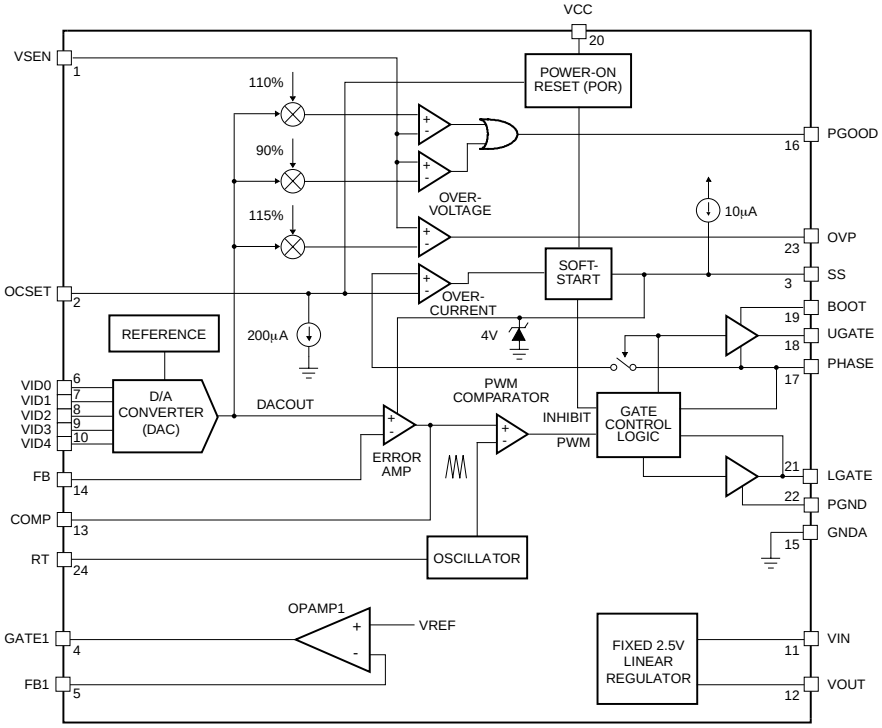
- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

The RC5055 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5055 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5055 uses a high level of integration to deliver load currents in excess of 17A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 50KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5055 also offers integrated functions including Power Good, Output Enable/ Soft Start, over-voltage protection and current limiting. The two linear regulators are also specified at 1% precision.

Preliminary Information

Block Diagram



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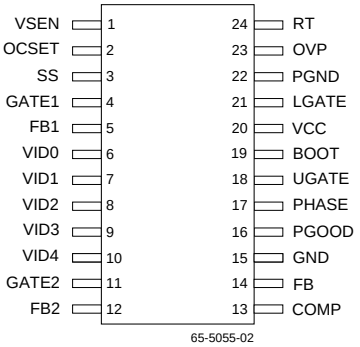
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	VSEN	This pin is connected to the converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
2	OCSET	Connect a resistor (ROCSET) from this pin to the drain of the upper MOSFET. An internal 200μA current source (Iocs) and the upper MOSFET $R_{DS(ON)}$ set the converter peak over-current trip point: $$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$$
3	SS	Soft Start. A capacitor from this point to ground together with an internal 10μA will cause the output duty cycle to increase slowly
4	GATE1	First LDO Error Amplifier Output.
5	FB1	First LDO Error Amplifier Inverting Input. When FB1 and GATE1 are tied together the Output Voltage = Vref
6-10	VID0-4	DAC inputs. Used to adjust the output voltage to the voltage required by the processor.
11	VIN	Second LDO Error Amplifier Output. Vout = Vref*(R1+R2)/R1
12	VOUT	Second LDO Error Amplifier Inverting Input.
13	COMP	PWM Loop Error Amplifier output.
14	FB	PWM Loop Voltage Feedback. Inverting input of Error Amplifier.
15	GND	Signal Ground.
16	PGOOD	Power good. This pin is pulled low when the converter output is not within 10% of the Dacout reference voltage.
17	PHASE	Connect the PHASE to the upper MOSFET source.
18	UGATE	Upper MOSFET gate driver
19	BOOT	Upper MOSFET bootstrap.
20	VCC	12V bias supply.
21	LGATE	Low MOSFET gate driver.
22	PGND	Power ground.
23	OVP	Over-voltage Protection. This pin drives an external SCR.
24	RT	Oscillator switching frequency adjust according to the following equations: $$F_S = 200KHz + 5.6\times10^3\frac{[KHz \times Kohm]}{R_t[Kohm]}$$ (RT to GND) $$F_S = 200KHz - 30\times10^3\frac{[KHz \times Kohm]}{R_t[Kohm]}$$ (RT to 12V)

Preliminary Information

Absolute Maximum Ratings

Parameter	Min.	Max.
Power Input Voltage, Vin		6V
Supply Voltage Vcc		13.5V
Boot Voltage, V_{BOOT}-V_{PHASE}		13.5V
I/O Voltages	GND-0.3V	Vcc+0.3V
ESD Classification		Class 2

Operating Conditions

Parameter	Min.	Max.
Supply Voltage	+12V -10%	+12+10%
Ambient Temperature	0°C	70°C
Junction Temperature	0°C	125°C

Thermal Information

Parameter	Conditions	Min.	Typ.	Max.
Thermal Resistance SOIC 24 pin package	With TBD in^2 of Copper			
Maximum Junction Temperature	Plastic Package			150°C
Storage Temperature		-65°C		150°C
Maximum Lead Temperature	Soldering 10 Seconds			300°C

Electrical Specifications

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
PWM Section						
VCC Supply Current						
Nominal Supply	I_{CC}	UGATE and LGATE Open	–	22	–	mA
Power-On Reset						
Rising VCC Threshold		V_{OCSET} = 4.5V	–	–	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.8	–	–	V
Rising V_{OCSET} Threshold			–	1.26	–	V
Oscillator						
Free Running Frequency	F_S	RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	–	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = OPEN	–	1.9	–	V_{P-P}
Reference and DAC						
DACOUT Voltage Accuracy			-1.0	–	+1.0	%
Error Amplifier						
DC Gain	A_{DC}		–	88	–	dB
Gain-Bandwidth Product	GBW		–	15	–	MHz
Slew Rate	SR	COMP = 10pF	–	6	–	V/μs

Preliminary Information

Electrical Specifications (continued)

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Gate Driver						
Upper Gate Source Current	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V	350	500	–	mA
Upper Gate Sink Current	I_{UGATE}	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Lower Gate Source Current	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	350	450	–	mA
Lower Gate Sink Current	I_{LGATE}	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
Over-Voltage Trip (V_{SEN}/DACOUT)			–	115	120	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
OVP Sourcing Current	I_{OVP}	V_{SEN} = 5.5V; V_{OVP} = 0V	60	–	–	mA
Soft Start Current	I_{SS}		–	10	–	µA
Power Good						
Upper Threshold (V_{SEN} /DACOUT)		V_{SEN} Rising	106	–	111	%
Lower Threshold (V_{SEN} /DACOUT)		V_{SEN} Falling	89	–	94	%
Hysteresis (V_{SEN} /DACOUT)		Upper and Lower Threshold	–	2	–	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -5mA	–	0.5	–	V
Adjustable Linear Regulator						
Output Voltage		Set by external resistors	1.3			V
Output Voltage Precision		I_{LOAD} = 50 mAto 5.4A V_{CC} = 12V ± 10% T_A = 0 to 70°C R_1 = TBD R_2 = TBD	-2		+2	%
Controller Output Current	GATE 1		20			mA
Output Transient Tolerance		50mA to 4.4 Amp Set by ESR of output caps	-135		135	mV
Bias Current	FB 1			1		µA
Feedback Voltage	FB 1			1265		mV
Fixed Linear Regulator						
Output Voltage	V_{OUT}	I_{LOAD} ≤ 120mA V_{CC} = 12V ± 10% V_{IN} ≥ 3.3V	2.375	2.5	2.625	V
Under Voltage Level				60%		%
Output Current	I_{OUT}	V_{CC} = 12V ± 10% V_{IN} = 3.3V		120		mA
Over Current Trip Point		V_{CC} = 12V ± 10% V_{IN} = 3.3V	150			mA
Input Voltage	V_{IN}	V_{CC} = 12V ± 10%	3.14	3.3	3.47	V

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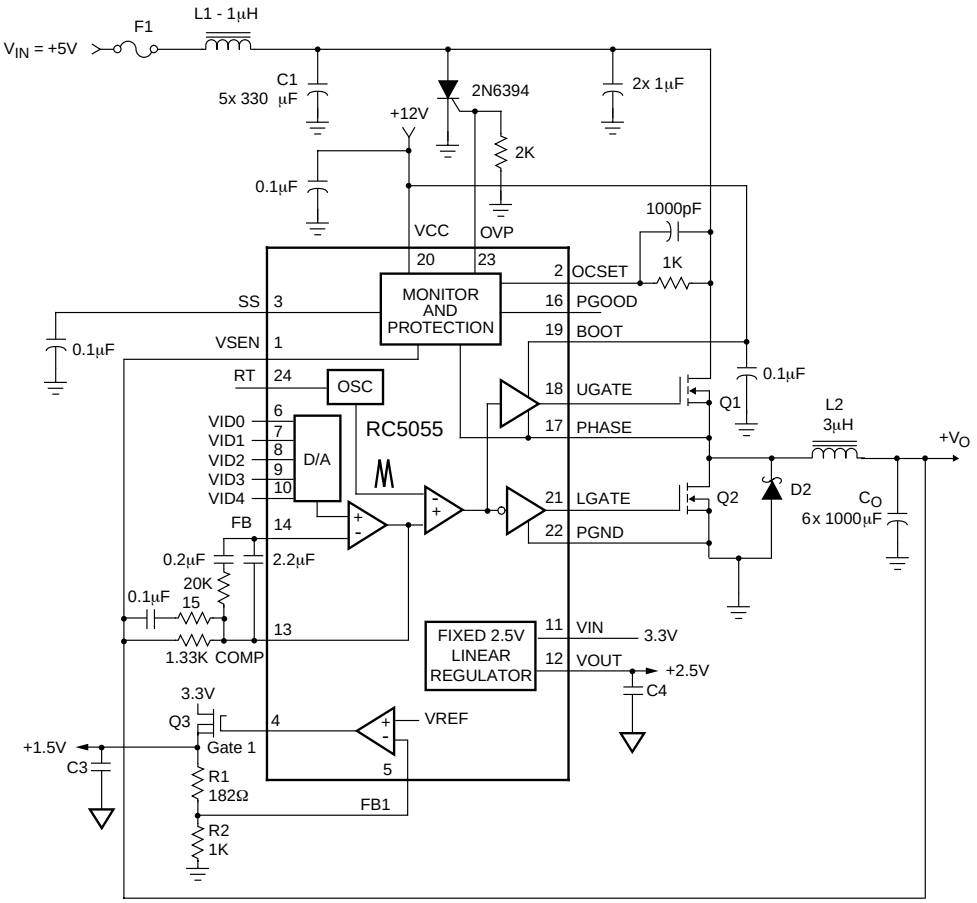


Figure 1. Pentium II DC-DC Converter

Table 1. Bill of Materials for Figure 1

Item	Quantity	Manufacturer	Part Number	Description
C0	6	Sanyo	MV-GX	1000µF 6.3 WVDC
C1	5	Sanyo	MV-GX	330µF 25 WVDC
C3	2	Sanyo	10MV1200GX	1200µF 10 WVDC
C4	1	AVX	TPSC107M0063R150	100µF 6.3 WVDC
R1	1	Generic		182Ω 1%
R2	2	Generic		1K 1%
L1	1	Micrometals	Core: T50-52	5 Turns of 18 AWG Copper Wire
L2	1	Micrometals	Core: T50-52B	5 Turns of 16 AWG Copper Wire
D1	1	Generic	1N4148	Diode
D2	1	Motorola	MBR340	Schottky Diode
Q1, Q2	2	Fairchild Semiconductor	NDB7030L	Power MOSFET
Q3	1	Fairchild Semiconductor	NDB4050	MOSFET $R_{DS(ON)}$ = 1Ω

Preliminary Information

The output voltage of a RC5055 converter is programmed to discrete levels between 1.3VDC and 3.5VDC . The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 2 specifies the DACOUT voltage for the 32 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection. The DAC function is a precision non-inverting summation amplifier shown in Figure 2. The resistor values shown are only approximations of the actual precision values used. Grounding any combination of the VID pins increases the DACOUT voltage. The 'open' circuit voltage on the VID pins is the band gap reference voltage, 1.26V.

Table 2. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	2.0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

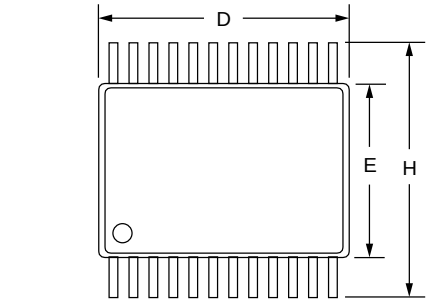
Package Dimensions

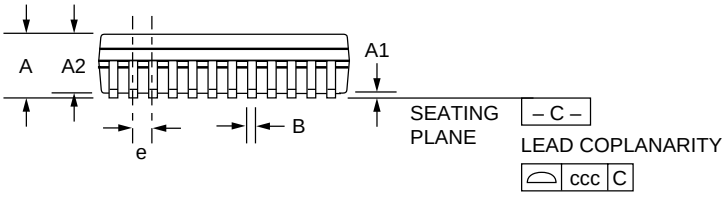
24-pin SSOP package

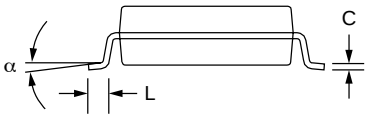
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.078	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.010	.015	0.22	0.38	5
c	.0035	.010	0.09	0.25	5
D	.311	.335	7.90	8.50	2, 4
H	.291	.323	7.40	8.20	
E	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







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Ordering Information

Product Number	Package
RC5055M	24 pin SSOP

Preliminary Information

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